

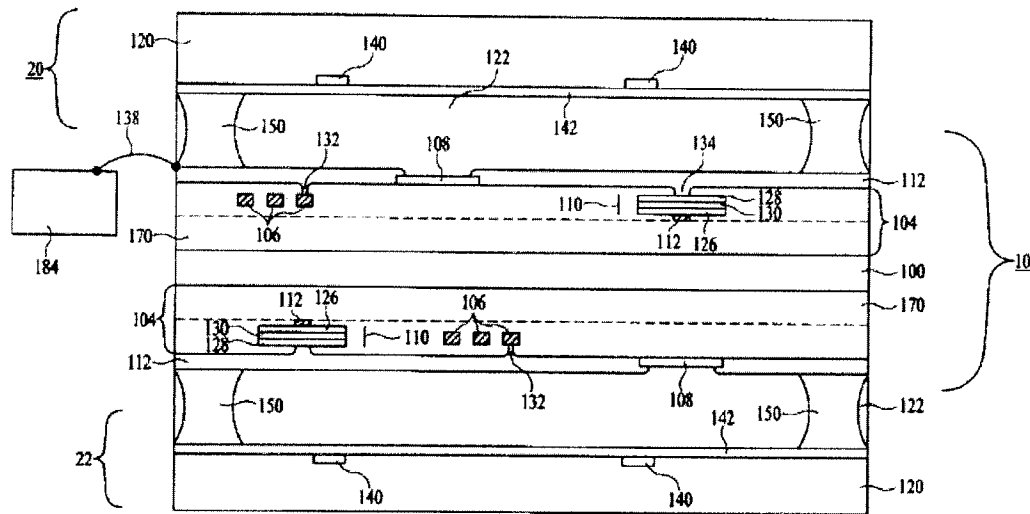
REMARKS

Claims 1 to 4 and 7 to 29 are pending, of which claims 1 and 26 are independent.

Favorable reconsideration and further examination are respectfully requested.

In the Office Action, claims 1 to 3, 10, 17, 18, 22, 23, and 25 to 27 were rejected over Ahn; claim 4 was rejected over Ahn and U.S. Patent No. 6,970,362 (Chakravorty); claims 5, 11, 12, 13, 15, 19, 20, 21 and 28 were rejected over Ahn and U.S. Patent No. 6,628,178 (Uchikoba); claim 6 was rejected over Ahn and U.S. Patent No. 6,673,697 (Ma); claim 7 was rejected over Ahn and U.S. Patent No. 6,713,860 (Li); claim 8 was rejected over Ahn and U.S. Patent No. 6,955,948 (Asahi); claim 9 was rejected over Ahn and U.S. Patent No. 6,388,207 (Figueroa); claim 14 was rejected over Ahn, Uchikoba and U.S. Patent No. 6,060,954 (Liu); claim 16 was rejected over U.S. Patent No. 6,642,811 (Daniels); and claim 29 was rejected over Ahn and U.S. Patent No. 6,356,453 (Juskey). As shown above, the claims have been amended. In view of these amendments, withdrawal of the art rejections is respectfully requested.

In this regard, Ahn shows an interposer 10 between two chips 120 above and below the interposer (see Fig. 1 of Ahn below). Interposer 10 was equated to the multi-layer substrate in the claims. We respectfully disagree, particularly in view of the claim amendments made herein.



In this regard, independent claims 1 and 26 recite that the multilayer substrate includes first external contacts on its underside, and that the at least one chip component includes second external contacts. The first external contacts are electrically connected to the second external contacts via an impedance conversion circuit, which comprises an inductive circuit, electrically connected in series between the first external contacts and the second external contacts. Ahn clearly does not disclose or suggest these features. In fact, Ahn teaches away from them.

More specifically, the interposer 10 of Ahn includes a substrate layer 100 and insulating layers 104 between the chips 120, thereby electrically isolating the chips 120 from each other. By contrast, in claims 1 and 26, the multilayer substrate acts as a path for electrically connecting external contacts of a chip and external contacts on an under side of the substrate. In this regard, interposer 10 does include inductors 106; however, these inductors are not in series between first external contacts of a chip component 120 and second external contacts on an underside of the substrate. Rather, inductors 106 are used for forming electrical connections between integrated

circuit elements 140 (parts of chip 120) on the *same side* of the interposer 10 (which is the alleged counterpart to the multilayer substrate of the claims.

We also note that Ahn does not disclose or suggest that its chip 120 comprise bulk or surface acoustic wave resonators, as claimed. In this regard, Ma does describe a mountable bulk acoustic wave (BAW) resonator. However, there is no disclosure or suggestion whatsoever to mount a BAW resonator, such as that shown in Ma, on interposer 10 of Ahn. For example, interposer 10 does not include an open area (such as area 38 of Ma) over which to place the membrane of BAW resonator 10. That is, area 122 of Ahn is epoxy and 150 are solder joints.

Uchikoba discloses a surface acoustic wave (SAW) resonator mounted on a substrate 40. However, Uchikoba does not disclose or suggest an impedance conversion circuit between external contacts of the SAW resonator and external contacts of the substrate. In this regard, Fig. 3 shows an inductor on a path to ground; however, that inductor appears to function as a ground connection (a shunt) and not as an impedance conversion circuit between an external contact of the SAW resonator and an external contact of the substrate.

The remaining art is likewise not understood to disclose or to suggest the foregoing features of the claims. Accordingly, claims 1 and 26 are believed to be patentable.

Each of the dependent claims is believed to define patentable features of the invention. Each dependent claim partakes of the novelty of its corresponding independent claim, in light of the foregoing amendments, and, as such, has not been discussed specifically herein.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above

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may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.


In view of the foregoing amendments and remarks, Applicant respectfully submits that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Please charge any additional fees, not already covered by check, or credit any overpayment, to deposit account 06-1050, referencing Attorney Docket No. 14219-075US1.

Applicant's attorney can be reached at the address shown above. Telephone calls regarding this application should be directed to 617-521-7896.

Respectfully submitted,

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